Q.P. Code: 18EC0402 **R18**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Supplementary Examinations August-2021

DIGITAL SYSTEM DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

PART-A

(Answer all the Questions **5 x 2 = 10** Marks)

1	a	Why XS-3 code is called a self complementing code?	**2M**
	b	List the applications of MUX and DEMUX.	**2M**
	c	Draw the MOD-2 Counter	**2M**
	d	Realize F(x,y,z) = Σm(1,2,5,7) using PLA.	**2M**
	e	Write a VHDL Program for 2x4 Decoder in Dataflow Model	**2M**

PART-B

(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2	a	Convert the following. i) (BC)16 = ( )10 ii) (2314)8= ( )10 iii) (1000011)2 = ( )10 iv) (647)10=( )16 v) (292)10 = (1204)b	**5M**
	b	Express the following numbers in decimal. (I) (10110.0101)2 (II) (16.5)16 (III) (26.24)8 (IV) (BC54)16 (V) (323)8	**5M**

OR

3	a	Explain about the Binary Codes.	**5M**
	b	Simplify the following Boolean functions to minimum number of literals. i) F=xy+x'z+yz. ii) F=x'y'z+x'yz+xy' iii) F= (x+y)'(x'+y') iv) F=xy+xy'+x'y v) F= (BC'+A'D)(AB'+CD')	**5M**

UNIT-II

4	a	Simplify the following Boolean function for minimal SOP & POS form using K-map F (A, B, C, D) = Σ (0,1,2,5,8,9,10)	**5M**
	b	Explain about carry look ahead adder with suitable diagram	**5M**

OR

5	a	Obtain Product of sums form for F=x'z'+y'z'+yz'+xy	**5M**
	b	With a neat design procedure, explain the implementation of a 4-bit Magnitude Comparator.	**5M**

UNIT-III

6	a	Explain the difference between Ring and Johnson counters with neat sketch	5M
	b	Explain the operation of an SR Flip Flop using excitation table. Give its Truth Table and Characteristic Equation	5M

OR

7	a	Design and implement a BCD Ripple counter using JK Flip Flops.	6M
	b	Give the characteristic table, Truth table, characteristic equation and excitation table for T and D Flip Flops.	4M

UNIT-IV

8	a	What is meant by Tristate logic? Draw the circuit of Tristate TTL logic and explain the functions.	6M
	b	Derive the PLA programming table for the combinational circuit that squares a 3-bit number.	4M

OR

9	a	Give the classification of integrated circuits and compare the various logic families	5M
	b	Compare three combinational circuits: PLA, PAL and ROM.	5M

UNIT-V

10	a	Explain the importance of Schematic in VHDL.	5M
	b	Write a VHDL program for a 4X1 MUX.	5M

OR

11	a	Explain about Simulation and Synthesis processes in VHDL	5M
	b	Write a VHDL program for 3 to 8 Decoder	5M

END